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1 INTRODUCTION

This document defines a list of requirements for a trusted environment, as defined by the OMTP Hardware Working Group.

Those requirements are formalizing the security needs of sensitive assets and applications, such as Debug Port protection, Secure Boot and Secure Flash update, Mobile device ID protection, SIM Lock protection, and DRM application.

Most of the requirements allow for the implementation solutions to differ amongst the players at the mobile platform level (semiconductor providers, software providers and platform integrators, and terminal manufacturers). As an illustration, the confidentiality of critical data can be achieved either by storing this data in encrypted form inside Non-Secure Memory or by storing this data in clear-text in Secure Memory or in Secure Hardware registers. In the latter case, as described in section 5.5, the confidentiality is guaranteed by the set of access control and authentication mechanisms implemented to read or write to the critical data. However, in some cases, when absolutely critical for the security of the overall trusted environment, implementation-level requirements are defined.

To clearly qualify the security requirements listed in this document, and for them to be commensurate to the threats, the security model, including the threat model and the trust model, is defined in section 5 “Security Model”. We therefore define:

1. Which categories of attacks must be taken into consideration
2. Which platform components are trusted to do what

Once threat and trust models are defined, requirements can be expressed in terms of security properties that SHALL be guaranteed within the given threat and trust model (or in other words which property of a given asset SHALL be ensured against the threat described in the threat model), without reference to the implementation solutions.

The requirements are separated in different sections:

- “General requirements”, listed in section 6
- “Debug Port Protection Requirements”, listed in section 7
- “Mobile Device ID Requirements”, listed in section 8
- “SIM Lock & ME Personalisation Requirements”, listed in section 9
- “DRM Requirements”, listed in section 10
- “Secure Boot Requirements”, listed in section 11

- “Secure Binding Requirements”, listed in section 12
- “Secure Flash Update Requirements”, listed in section 13

These requirements are defined as part of the Profile TR 0, which is currently the only profile defined. Further profiles will be added in future version of the documents.

Profile TR 0 has two sub profiles, named TR 0.1 and TR 0.2. The requirements encompassed by these two sub-profiles are the following:

For TR 0.1: it SHALL support the following sections:

- Requirements listed in General Requirement section (both General Requirement and Hardware Unique Key parts)
- Requirements listed in Debug Port section
- Requirements listed in Mobile Device ID section
- Requirements listed in SIM-Lock & ME Personalisation section
- Requirements listed in Secure Boot section
- Requirements listed in the Secure Binding section

and MAY support following:

- Requirements listed in Secure Flash Update section

For TR 0.2: it SHALL support the following sections:

- Requirements listed in General Requirement section (both General Requirement and Hardware Unique Key parts)
- Requirements listed in Debug Port section
- Requirements listed in Mobile Device ID section
- Requirements listed in SIM-Lock section
- Requirements listed in DRM section
- Requirements listed in Secure Boot section
- Requirements listed in the Secure Binding section

and MAY support following:

- Requirements listed in Secure Flash Update section

1.1 DOCUMENT PURPOSE

This document has a general objective to help in defining terminal requirements and to allow development and deployment of new

services as well as de-fragmenting secure requirements offered within terminals.

In particular, the document concurs to the main OMTP objectives:

Facilitate implementation of Open Mobile Terminal Platforms

- Work as appropriate to drive specific mobile terminal platforms to meet OMTP requirements
 - Influence standardization of relevant platforms;
 - Work with Vendors of proprietary platforms to adopt requirements and/or resulting standards
- Understand implementation roadmap and conformance to requirements

In particular it addresses the hardware enablers through the production chain to facilitate terminal development.

Define De-Fragmentation Guidelines

- De-fragmentation guidelines to reduce costs (both for operators and manufacturers) and increase consistency by defining
 - hardware component parameters;
 - software component parameters;
 - performance guidelines & benchmarks

1.2 INTENDED AUDIENCE

The document is intended to be used as reference in:

- terminal requirements definition,
- platform and terminal characteristics description,
- to refer to secure hardware in mobile terminal definition

Some examples of usage follow:

Within hardware requirements for an application: “The terminal needs an IMEI protection compliant with OMTP profile TR 0.1 definition as defined in ‘OMTP hardware requirements and defragmentation: Trusted environment – OMTP TR 0’”

In order to deliver the right level of security for this content delivery solution, DRM agent and related applications shall be based on an architecture compliant with the OMTP requirements as defined in the profile TR 0.2/DRM section of the ‘OMTP hardware requirements and defragmentation: Trusted environment – OMTP TR 0’.

1.3 DEFINITIONS

As defined in 3GPP TR 21.905 [2] standard, we will refer to **User Equipment (UE)** as a device allowing a user access to network services. For the purpose of 3GPP specifications the interface between the UE and the network is the radio interface. A User Equipment can be subdivided into a number of domains, the domains being separated by reference points. Currently defined domains are the **Subscriber Identity Module (SIM)/ Universal Subscriber Identity Module (USIM)** and **Mobile Equipment (ME)** Domains.

We will refer to (U)SIM as SIM, USIM or UICC without distinction (named (U)SIM in this document) unless it makes sense to do otherwise, in which case the specific usage domain shall be used.

The SOC (System On Chip) encompasses the chip(s) handling the application plus the modem communication processing, i.e. digital base bands with optional additional application processors.

2 CONVENTIONS

The key words “MUST”, “MUST NOT”, “REQUIRED”, “SHALL”, “SHALL NOT”, “SHOULD”, “SHOULD NOT”, “RECOMMENDED”, “MAY”, and “OPTIONAL” in this document are to be interpreted as described in RFC2119 [1].

- **MUST:** This word, or the terms "REQUIRED" or "SHALL", mean that the definition is an absolute requirement of the specification.
- **MUST NOT:** This phrase, or the phrase "SHALL NOT", mean that the definition is an absolute prohibition of the specification.
- **SHOULD:** This word, or the adjective "RECOMMENDED", mean that there may exist valid reasons in particular circumstances to ignore a particular item, but the full implications must be understood and carefully weighed before choosing a different course.
- **SHOULD NOT:** This phrase, or the phrase "NOT RECOMMENDED" mean that there may exist valid reasons in particular circumstances when the particular behaviour is acceptable or even useful, but the full implications should be understood and the case carefully weighed before implementing any behaviour described with this label.
- **MAY:** This word, or the adjective "OPTIONAL", mean that an item is truly optional. One vendor may choose to include the item because a particular marketplace requires it or because the vendor feels that it enhances the product while another vendor may omit the same item. An implementation which does not include a particular option **MUST** be prepared to interoperate with another implementation which does include the option, though perhaps with reduced functionality. In the same vein an implementation which does include a particular option **MUST** be prepared to interoperate with another implementation which does not include the option (except, of course, for the feature the option provides.)

3 ABBREVIATIONS

ABBREVIATION	DESCRIPTION
3DES	Triple Data Encryption Standard
AES	Advanced Encryption Standard
CDMA	Code Division Multiple Access
CK	Control Key
DRM	Digital Rights Management
EEPROM	Electrically Erasable Programmable Read Only Memory
EMA	Electro Magnetic Analysis
ESN	Electronic Serial Number
FIB	Focussed Ion Beam
GPS	Global Positioning System
GSM	Global System for Mobile communications
HMAC	Hash Message Authentication Code
HW	Hardware
HU	Hardware Unique key
ID	Identifier
IR	Infrared
IRDA	Infrared Data Association
IMEI	International Mobile Equipment Identifier
JTAG	Joint Test Action Group
ME	Mobile Equipment
OMTP	Open Mobile Terminal Platform
OS	Operating System

ABBREVIATION	DESCRIPTION
PCK	Personalisation Control Key
PKI	Public Key Infrastructure
PROM	Programmable Read Only Memory
PRNG	Pseudo Random Number Generator
RAM	Random Access Memory
RF	Radio Frequency
RNG	Random Number Generator
ROM	Read Only Memory
RSA	Rivest Shamir Adleman: a Public Key cryptography standard, named after its inventors, that can be used both for encrypting messages and making digital signatures
SIM	Subscriber Identity Module
SHA	Secure Hash Algorithm
SOC	System On Chip
SW	Software
TR	Trusted Environment
UE	User Equipment
UICC	Universal Integrated Circuit Card
UMTS	Universal Mobile Telecommunications Service
USIM	Universal Subscriber Identity Module

Each requirement listed in the tables in this document has a single reference which includes an ID tag and the number of the requirement in the table. The ID tags are listed below:

ABBREVIATION	DESCRIPTION
DP	Debug Port Requirement
DRM	DRM Requirement
GR	General Requirement
HU	Hardware Unique Key Requirement
IM	Mobile Device ID Requirement
SB	Secure Boot Requirement
SG	Secure Binding Requirement
SF	Secure Flash Update Requirement
SL	SIM-Lock Requirement

4 REFERENCED DOCUMENTS

No.	DOCUMENT	AUTHOR	DATE
1	RFC 2119 - Key words for use in RFCs to Indicate Requirement Levels (http://rfc.net/rfc2119.html)	IETF documents	March 1997
2	3GPP TR 21.905 V7.0.0	3GPP	September 2005
3	EICTA CCIG Doc Ref: Eicta Doc: 04cc100 GSMA Doc Ref: Security Principles Related to Handset Theft 3.0.0	EICTA CCIG & GSMA	
4	3GPP TS 23.003 v.6.8.0	3GPP	September 2005
5	3GPP TS 22.022 V6.0.0	ETSI	December 2004
6	FIPS 140-2. http://csrc.nist.gov/publications/fips/fips140-2/fips1402.pdf	NIST	

5 SECURITY MODEL

The purpose of developing a security model for a UE is to provide a framework for discussing security mechanisms that are intended to enforce a security policy describing the protection of certain assets against threats that are assumed to be present in the UE's environment. Accordingly, the following subsections of this security model define the UE, its environment, the assets to be protected, the assumed threats and a trust model for describing appropriate security policies. The requirements for any particular service detailed in this document are only applicable if the target terminal supports the intended service. Applicable service features may vary depending on the terminal category.

5.1 UE MODEL

This security model concerns mobile communication and information processing UEs that connect to one or more commercial telecommunications networks. Typically this is a handheld, battery-powered electronic UE that provides voice and/or data communication services to an individual user. The UE may optionally provide data storage and offline information processing capabilities for the user. The UE generally contains one or more microprocessors, volatile RAM and non-volatile storage that are electronically accessible to those microprocessors, and the necessary RF electronics to communicate via a standard wireless telecommunication network such as GSM or UMTS as well as interfaces toward (U)SIM. The UE may also be capable of communicating over RF or IR interfaces that are not part of a standard wireless telecommunication network (e.g.; Bluetooth, IEEE 802.11, IRDA). Typically the UE will incorporate a speaker and microphone that allow a user to conduct voice communications, but these facilities may optionally be provided via wired or wireless interfaces to a separate headphone and microphone. The UE may contain a digital display, a keypad and various other buttons, a slot for removable non-volatile media, a digital interface port, a camera, a GPS unit, or other consumer electronics features. The microprocessors within the UE execute software that implements various features of the UE, usually including the communications protocols appropriate to the wireless telecommunications network. The UE boots up by first executing software resident in non-volatile memory, but may thereafter execute software from volatile RAM. The same microprocessor may execute both telecommunications software and applications software that is not related to telecommunications.

5.2 (U)SIM

Referred also as SIM, the UE incorporates a (U)SIM being the trusted-by-operator module. The (U)SIM contains a trusted-by-operator execution environment and a trusted-by-operator memory. The (U)SIM is a tamper-resistant device, i.e., it is resistant to invasive attacks, fault attacks and side channel analysis. The (U)SIM communicates with the UE through its interface.

The (U)SIM is issued by the operator as:

- Operator security module
- User Identification module

5.3 UE ENVIRONMENT

Legitimate UEs will be manufactured and initially provisioned in facilities that guarantee that the hardware, software, configuration and authentication data installed in the UEs are authentic and uncorrupted. However, UEs will be distributed and used in environments which do not guarantee that the hardware, software, configuration and authentication data remain unmodified from their original state. The UE's keyboard, other buttons, non-volatile storage port, headset interface, and (U)SIM contacts are accessible by the user, and by persons in the distribution chain. A person with physical access to the UE could partially disassemble the UE to expose internal interfaces. Even without physical contact, the UE's wireless interfaces, including RF, IR and Bluetooth ports, are potentially accessible whenever the UE is powered on.

5.4 ASSETS

Security issues connected with mobile telecommunications UEs are related to the fact that the UE has associated assets that must be protected. Some of these assets are:

- The software installed on the UE by the manufacturer
- The software installed on the UE by the operator
- The software and the information residing on the (U)SIM
- Other information assets include data stored on the UE by the user, which may be software, personal or corporate data (e.g. password, electronic certificate for remote access to extranets), ringtones, music, or video that the user has purchased from the telecommunications carrier or a third party.

Some data stored on the UE, such as cryptographic keys, represent more abstract assets, such as rights to access communication services, credit card accounts, private address books, etc. In many

cases, preserving the value of the information asset requires that the confidentiality and/or integrity of the asset be maintained. In some cases the authenticity of the information asset must be ascertained.

5.5 THREAT MODEL

The following attacks are to be addressed and considered in the scope of the threat model:

- Attacks from Non-Secure SW
- Inter-chip signal probing attacks
- Board level SW-based Debug and Test attacks
- Attacks via external physical interfaces
- Memory or data storage elements that are replaceable without the destruction of the UE
- Removal or substitution of any HW elements that are (1) not part of the processor's SOC physical package and (2) replaceable without the destruction of the UE (e.g. unsoldering attacks)
- Off-line modification of the contents of non-volatile storage mechanisms (e.g. Flash, EPROM)

The following attacks are not to be addressed and considered out of the scope of the threat model:

- Chip-Level HW attacks (on-chip probing, FIB, etc)
- Other hardware removal or substitution attacks not defined above
- Side-channel attacks (power, timing, EMA, etc.)
- Board-level inter-chip bus write attacks on RAM or FLASH memories whilst the SOC is powered
- Fault attacks (such as glitch, light, laser, etc.) are attacks relying on physical perturbation to introduce fault in the software execution and then exploit the faults induced in the software to override security measures

Board-level or SW-based Debug and Test attacks have to be considered within the threat model. However, given the intrinsic intrusive nature of these debug features, such attacks must be countered via specific requirements related to the implementation of the debug port. These requirements are detailed in section 7 "Debug Port Protection Requirements".

5.6 TRUST MODEL & DEFINITIONS

5.6.1 DEFINITIONS OF SECURITY PROPERTIES

Authenticity: the quality of an asset of being authentic and attributable to its authors or caretakers.

Integrity: the quality of an asset of being genuine or not corrupted from the original.

Confidentiality: the quality of an asset of only being readable by those authorized to do so.

Authorized Party: refers to an entity that has been accredited to perform sensitive operations. The particular entity that is accredited depends on the security policy of the operator (e.g. it can be the ME provider, the operator, a distributor or even the user).

5.6.2 DEFINITIONS OF HW RESOURCES

In this document, when we refer to components that are OS-Controlled, Closed/Secure OS-Controlled, or HW-Controlled, it means that those components are controlled as defined hereafter:

- OS-Controlled component: A component to which the access and use is enforced by a mechanism under OS control.
- Closed/Secure OS-Controlled component: A component to which the access and use is enforced either by:

(a) a closed OS which has been configured not to allow installation of non-sandboxed or native executables after manufacture except where such executables are supplied by the device manufacturer in a secure manner, to allow access to HW resources from execution environments running in the OS

(b) An OS which allows installation of non-sandboxed or native executables after manufacture but which supports mechanisms to forbid access to HW resources from the application framework and from execution environments running in the OS and where the HW resources can only be accessed by a small subset of the APIs of the OS, where these APIs can only be called by software authorised by the Manufacturer.

- HW-Controlled component: A component to which the access and use is enforced by a hardware mechanism not under OS control. HW-Controlled assets or mechanisms are protected against attacks on or through the application framework and against attacks on the OS (typically attacks leveraging OS bugs and other vulnerabilities, such as buffer overflow attacks).

- **Integrity-Protected HW:** HW that is integrity-protected against the kind of attacks described in the threat model.
- **Confidentiality Protected HW:** HW that is confidentiality-protected against the kind of attacks described in the threat model.
- **Secure HW:** HW that is integrity-protected and confidentiality-protected against the kind of attacks described in the threat model.
- **Secure Memory:** Any memory that is integrity-protected and confidentiality-protected against the kind of attacks described in the threat model. The level of protection against software attacks depends on how the access to the memory is controlled:
 - **OS-Controlled Secure Memory:** Secure Memory whose access is controlled by the OS.
 - **Closed/Secure OS-Controlled Secure Memory:** Secure Memory whose access is controlled by a Closed/Secure OS.
 - **HW-Controlled Secure Memory:** Secure Memory whose access is controlled by HW mechanisms and not under the control of the main OS.
- **Integrity-Protected Memory:** Any memory that is integrity-protected against the kind of attacks described in the threat model. The level of protection against software attacks depends on how the access to the memory is controlled:
 - **OS-Controlled Integrity-Protected Memory:** Integrity-Protected Memory whose write access is controlled by the OS.
 - **Closed/Secure OS-Controlled Integrity-Protected Memory:** Integrity-Protected Memory whose write access is controlled by a Closed/Secure OS.
 - **HW-Controlled Integrity-Protected Memory:** Integrity-Protected Memory whose integrity is either intrinsically guaranteed or whose write access is controlled by HW mechanisms and not under the control of the main OS.
- **Integrity-Checked Memory:** Any memory whose integrity is checked at run-time, but not necessarily before every memory access. There can be a delay between the time when the memory integrity is compromised and the time of detection. It could be classified between:

- **OS-Integrity-Checked Memory:** Integrity-Checked Memory whose integrity is checked by the OS.
- **Closed/Secure OS-Integrity-Checked Memory:** Integrity-Checked Memory whose integrity is checked by a Closed/Secure OS.
- **HW-Integrity-Checked Memory:** Integrity-Checked Memory whose integrity is checked by HW mechanisms.

Note:

- The way the check is performed at run-time shall be specified in the requirement.
- OS-Integrity-Checked, Closed/Secure OS-Integrity-Checked and HW-Integrity-Checked Memories are generally external accessible memories exposed to board level attacks.

Since there can be a delay between the time when the memory integrity is compromised and the time of detection, corrupted code or data may be used.

- **Non-Secure Memory:** memory that does not belong to the previous categories.

5.6.3 DEFINITIONS OF SOFTWARE

- **Authenticated SW:** authenticated and integrity-checked SW. Authenticity and integrity can be either an intrinsic property of its storage (in the case of SW stored in an embedded ROM) or explicitly verified.
- **Authorized SW:** Authenticated SW with specific (intrinsic or granted) access privileges towards a particular function / resource.
- **Protected SW:** Authorized SW whose security properties (integrity, authenticity and privileges) are verified and enforced.
 - **OS-Protected SW:** Authorized SW whose security properties (integrity, authenticity, and privileges) are verified and enforced by the OS at run-time.
 - **Closed/Secure OS-Protected SW:** Authorized SW whose security properties (integrity, authenticity and privileges) are verified and enforced by a Closed/Secure OS at run-time.

- **HW-Protected SW:** Authorized SW whose security properties (integrity, authenticity, privileges) are either intrinsic properties or ensured by HW mechanisms and can not be compromised by OS-level software attacks, including OS kernel mode attacks.

Note: Protected SW may not be protected against board level attacks depending on the type of memories it is using and operating from.

- **Non-Secure SW:** SW that does not belong to the previous categories.

5.6.4 DEFINITION OF (U)SIM RELATED RESOURCES

- HW contained in a (U)SIM is considered
 - Secure HW
- (U)SIM OS is considered
 - Closed/Secure OS
- The memory contained in a (U)SIM is considered as all of
 - HW-Controlled Secure Memory
 - Closed/Secure OS-Controlled Secure Memory
 - HW-Integrity-Checked Memory
- Software running in a (U)SIM is considered as all of
 - HW-Protected SW
 - Close/Secure OS-Protected SW

If a secure binding among (U)SIM and ME microprocessor is in place, (U)SIM and ME microprocessor are considered in the same secure execution domain.

6 GENERAL REQUIREMENTS

The requirements here below are common to all use cases that need to use these particular functions.

6.1 GENERAL REQUIREMENTS

REQ. ID	REQUIREMENT
GR 1	The Manufacturer SHOULD promptly investigate reported weaknesses in the security of MEs and SOCs and SHALL address discovered weaknesses in future versions of the ME or SOC as soon as reasonably possible.
GR 2	The compliant party (e.g. the ME manufacturer, the (U)SIM manufacturers etc.) SHOULD provide documentation to interested operators to declare and explain how solutions implement the requirements in this document.

6.2 HARDWARE UNIQUE KEY REQUIREMENTS

HU 1	The ME SHALL support a unique ME specific key (Hardware Unique Key – HU key) used for internal security mechanisms.
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HU 2	<p>The generation of the HU key, if performed within the ME, SHALL be performed using hardware true random number generation in Secure HW or using pseudo-random number generation. The pseudo-random number generator SHALL use only secure HW, HW-Controlled Secure Memory and HW-Protected SW executing from HW-Controlled Integrity-Protected Memory. If performed outside of the ME, either a hardware true random number generator or a pseudo-random number generator SHALL be used. In all cases where the HU key is generated by pseudo-random number generation, a well-seeded cryptographic quality pseudo-random number generator SHALL be used. If the random key is generated outside of the ME, it SHALL be loaded into the ME in secure conditions.</p> <p>Note: When saying that a pseudorandom number generator (PRNG) is "well-seeded", it means that it is initialised with genuinely unpredictable information with sufficient entropy that an attacker cannot guess the seed any more efficiently than he could guess values produced by the PRNG. So for example a PRNG producing 128-bit "random numbers" should be initialised with at least 128 bits of entropy. A FIPS 140-2, section 4.7.1 ([6]), compliant random number generator fulfils this requirement.</p>
HU 3	Once the HU key has been generated by or loaded into the hardware it SHALL NOT be possible to change this key by any attack in the threat model.
HU 4	The HU key SHALL be stored in Secure HW or in HW-Controlled Secure Memory and SHALL only be accessible to Secure HW or to HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory.
HU 5	It SHALL NOT be possible to externally read out the HU key from the ME.
HU 6	The length of the HU key SHALL be at least 128 bits.
HU 7	The HU key SHALL only be used with established algorithms and techniques that will not compromise the security of the HU key at best of current knowledge.

HU 8	The HU key SHOULD only be used to protect or securely derive further keys (which are then used for functions within the ME) and SHOULD NOT be used directly by any function (aside from key protection or derivation) within the ME.
HU 9	With respect to requirements in this specification: Data cryptographically protected for confidentiality SHALL be protected by a cryptosystem providing the mathematical security strength at least equivalent to the AES algorithm using a 128-bit symmetric key or to 3DES algorithm using a 112-symmetric key.
HU 10	With respect to requirements in this specification: Data cryptographically protected for integrity SHALL be protected by a cryptosystem such that the mathematical complexity for generating data with the same digest as the protected data SHOULD be at least equivalent of Order of (2^{128}) or SHA-1's second pre-image resistance.
HU 11	With respect to requirements in this specification: Data cryptographically protected for authenticity SHALL be protected by a cryptosystem providing the mathematical security strength at least equivalent to an RSA signature algorithm using 1024-bit modulus and a SHA-1 message digest or to a HMAC SHA-1 using a 128-bit symmetrical key.

7 DEBUG PORT PROTECTION REQUIREMENTS

7.1 DESCRIPTION

Definitions:

- **Debug Port:**

A debug port allows external hardware and software test fixtures to connect to ME debugging software components and SOC on chip debugging support logic.

Debug ports can be classified as follows:

- **Software Implemented Debug Port:**

This is a facility implemented in ME software which exposes information about the internal state of the ME software running on the device and may allow the manipulation of such state over an interface of the device. Such a port may implement any of the Debug Port features.

Any interface on the device may be used for this purpose and its use as a debug port may not exclude its use as a port for other purposes.

It is the flow of debug information which has to be controlled - any other use of the interface should be unaffected.

- **Hardware Implemented Debug Port:**

This is a facility implemented in ME hardware which provides Debug Port features without the support of ME software.

The debug port in this case is typically dedicated to providing the debug capabilities. If the port is not dedicated, then the debug port information is carried on a channel over a shared physical port and such sharing is controlled by hardware.

It is this channel of information that has to be controlled e.g. Joint Test Action Group (JTAG) and multiplexed signalling.

A Hardware Implemented Debug Port: is a physical port (e.g. IEEE 1149.1, also known as JTAG), that connects external hardware and software test fixtures to on-chip debugging support logic providing (but not limited to) one of the features listed below:

Debug Port features:

Debug ports typically provide one or more of the features listed here below.

RUN-TIME CONTROL	Run-time control allows an external debug tool to start and stop the ME processor, to modify registers and to single-step (execute a single assembly instruction).
MEMORY ACCESS	Memory access allows an external debug tool to read and write memory. The access can be either normal access or on-the-fly access in which case the access is performed while the processor is running.
BREAKPOINTS	Breakpoints allow an external debug tool to halt execution when a specified event (breakpoint) has occurred. The event can be specified as code execution at a specified address or as a data access (read or write) to a specified address with a specified value. Watchpoints are a similar concept, however, when a watchpoint occurs a message is sent to the debug tool (as opposed to halting the processor).
INSTRUCTION OR PROGRAM TRACE	This feature allows an external debug to trace program execution and by this having full reconstruction of the program flow.
DATA TRACE	This feature allows an external debug tool to track real-time data accesses to memory locations.
OWNERSHIP TRACE	The Ownership Trace feature allows an external debug tool to identify (real-time) the currently executing process or task of an OS.
MEMORY SUBSTITUTION AND PORT REPLACEMENT	This feature allows internal memory or port accesses to be implemented over the auxiliary debug port. For example, this feature can be used to implement ROM patching, that is, instead of reading on-chip ROM, the instruction will be fetched from the debug tool via the auxiliary debug port.

The debug port protection requirements are formally defined within section 7.2. The following paragraphs provide an explanation for the debug port protection and the different debug port usage.

Debug port manipulation is one of the ways of executing unauthorized program code; getting control over the secure applications and/or running their code in privileged modes. The ME debug port generally provides access to all internal ME resources and interfaces, including the ME core and the system bus. This allows program control and visibility into ME program and data assets. Unprotected debug ports can be used to reconfigure protected data to permit the theft of services and ME cloning.

Debug ports such as the IEEE standard 1149.1 (also known as JTAG), may provide a hacker with all the means needed to break the system's security mechanisms and gain control over the operating system. Unauthorized debug port usage should be strictly forbidden in order to properly secure the ME. The ME debug port could however be accessible during platform initial laboratory bring-up, manufacturing, testing, and troubleshooting, as well as for software debugging by an authorized party. To properly secure the ME, all other accesses to the debug port should be strictly forbidden.

Application Specific debug facilities such as those being used by a Java developer towards the Java environment are not addressed by the Debug port protection requirements.

7.2 **DEBUG PORT REQUIREMENTS**

This section defines requirements for the SOC debug port.

REQ. ID	REQUIREMENT
DP 1	<p>Any unauthorized access to debug port features SHALL be prevented by the SOC. Only the terminal manufacturer or their delegates SHALL issue debug authorization. The terminal manufacturer can then further delegate the rights for subsequent delegation to other organizations.</p> <p>Blocking all debug port accesses, whether it is an authorized access or a non-authorized access, will be considered as satisfying this requirement.</p>

REQ. ID	REQUIREMENT
DP 2	A SOC incorporating an active Hardware Implemented Debug Port SHALL include support for an authentication mechanism that prevents unauthorized access to debug port services.
DP 3	This debug port protection mechanism itself SHALL be a SOC integrated HW mechanism. It SHALL be protected against any debug port manipulation that could subvert the authentication process. The authentication mechanism and the debug port control mechanism SHALL be handled either by Integrity-Protected HW or by HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory.
DP 4	An ME whose software implements a Software Implemented Debug port, SHALL have an authentication mechanism that prevents unauthorized usage of the debug port services. The authentication mechanism SHALL be handled by Protected SW executing from Integrity-Protected Memory, and using Secure Memory.
DP 5	The authorization to open the access to the debug port SHALL be uniquely associated with a given SOC.

8 MOBILE DEVICE ID REQUIREMENTS

8.1 DESCRIPTION

This section defines design and policy requirements intended to protect the Mobile Device ID assigned to a specific Mobile Equipment (ME), against modification and unauthorized manipulation of any kind. The main objective of these requirements is to establish trust in the Mobile Device ID value from the point of view of the software that is using it (typically: the GSM/GPRS/EDGE/UMTS protocol stacks), so that this software can be reasonably sure that the Mobile Device ID it uses is the one that has been assigned by recognized authorities to the Mobile Equipment running this software.

Thus, in the following, we highlight the fact that the authenticity, integrity and unique association (also called binding) between the Mobile Device ID and the ME (mainly represented by its hardware) are the main security properties of the Mobile Device ID asset to protect.

Definitions:

- **Mobile Device ID:** Defines the IMEI for GSM/UMTS devices or the ESN for CDMA devices.
- **Mobile Device ID Protection Mechanism:** It is intended to check the authenticity and the integrity of the **Mobile Device ID** value, the unique association of the **Mobile Device ID** to the ME, to detect modifications and to react to them.
- **IMEI:** The International Mobile Equipment Identity Number (IMEI) is a unique number given to every single terminal typically behind the battery. IMEI numbers of cellular phones connected to a GSM network are stored in a database register showing the allocation to a particular manufacturer for use with a particular model. The uniqueness of the IMEI identifying individual MEs allows access control of MEs by 3GPP networks. The IMEI is used for security purposes in case of theft or technical problems with a mobile network. When a mobile phone is reported stolen or is not type approved, the number is marked invalid.
- **ESN:** The Electronic Serial Number (ESN) is a unique identifier attached to MEs for cellular, personal communications and other wireless services that conform to a family of standards like AMPS, CDMA and TDMA in the United States. It corresponds to the IMEI.

8.2 MOBILE DEVICE ID REQUIREMENTS

MOBILE DEVICE ID AND BINDING OF THE MOBILE DEVICE ID:	
REQ. ID	REQUIREMENT
IM 1	Each ME SHALL be assigned a valid and unique Mobile Device ID before or upon its issuance AND in the particular case of GSM/UMTS devices as referred in the 3GPP TS 23 003 specification [4].
IM 2	The industrial process of binding the Mobile Device ID to the ME (Mobile Device ID assignment phase) SHALL be done by Authorized Parties, using appropriate security procedures.
IM 3	It SHALL not be possible for a ME to be assigned another Mobile Device ID after issuance.
IM 4	The ME SHALL ensure the authenticity and integrity of the Mobile Device ID as well as the binding of the Mobile Device ID with the ME.
IM 5	Unless the Mobile Device ID integrity and binding to the ME are protected using Integrity-Protected HW, the ME SHALL detect at boot-time and SHOULD detect at run-time, any modification of the Mobile Device ID or of the binding of the Mobile Device ID with the ME using the Mobile Device ID Protection Mechanism.
IM 6	<p>If the Mobile Device ID or the binding of the Mobile Device ID with the ME has been tampered with, before boot-time or at run-time, the ME SHALL NOT:</p> <ul style="list-style-type: none"> • be allowed to make any phone call nor any other network connection where the Mobile device ID is involved • communicate the modified Mobile device ID to the software components of the ME that use the Mobile device ID and rely on it; in particular, the Mobile device ID SHALL NOT be communicated to entity outside the ME.

MOBILE DEVICE ID AND BINDING OF THE MOBILE DEVICE ID:	
REQ. ID	REQUIREMENT
IM 7	In the particular case of GSM/UMTS devices, the ME SHALL be compliant with EICTA/GSMA recommendations: Security Principles Related to Handset Theft 3.0.0. [3].

SW COMPONENTS THAT USE THE MOBILE DEVICE ID AND THAT RELY ON IT:	
REQ. ID	REQUIREMENT
IM 8	SW components that report the Mobile device ID to the network SHALL be checked at boot time for authenticity and integrity as specified in section 11 "Secure Boot Requirements".
IM 9	If any modification of the SW components of the ME that report the Mobile device ID to the network is detected at boot time, the ME SHALL NOT be allowed to make any phone call nor any other network connection.

MOBILE DEVICE ID PROTECTION MECHANISM:	
REQ. ID	REQUIREMENT
IM 10	Mobile device ID Protection Mechanism SHALL be checked at boot time for authenticity and integrity as specified in section 11 "Secure Boot Requirements".

MOBILE DEVICE ID PROTECTION MECHANISM:	
REQ. ID	REQUIREMENT
IM 11	<p>In the case where it does not manipulate secrets, the Mobile device ID Protection Mechanism SHALL be either</p> <ul style="list-style-type: none"> • an Integrity-Protected HW, OR • a Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Protected Memory, OR • a HW-Protected SW executing from and using HW-Controlled Integrity-Protected Memory. <p>In the case where it manipulates secrets, the Mobile device ID Protection Mechanism SHALL be either</p> <ul style="list-style-type: none"> • a Secure HW ,OR • a Closed/Secure OS-Protected SW executing from Closed/Secure OS-Controlled Integrity-Protected Memory and using Closed/Secure OS-Controlled Secure Memory, OR • a HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory.
IM 12	<p>If any modification of the Mobile device ID Protection Mechanism is detected either at boot or at run-time, the ME SHALL NOT be allowed to make any phone call (including emergency calls) nor any other network connection where the Mobile device ID is involved.</p>

9 SIM LOCK AND ME PERSONALISATION REQUIREMENTS

9.1 DESCRIPTION

This section defines the requirements to guarantee security of the SIM-Lock Mechanism, the ME De-Personalisation Process, and of the ME Personalisation Information.

The requirements here below have been built in accordance with 3GPP TS 22.022 V6.0.0 [5]

Definitions:

- ME Personalisation Information:

3GPP TS 22.022 V6.0.0 [5] specifies five Personalisation categories of varying granularity:

- Network Personalisation
- Network Subset Personalisation
- Service Provider Personalisation
- Corporate Personalisation
- (U)SIM Personalisation

The ME Personalisation Information restricts the Network, Network Subset, Service Provider, and Corporate entities that the ME can connect to and also restricts the (U)SIM cards that can be used with the ME.

The ME can be personalized to one Network, one Network Subset, one Service Provider, one Corporate, one (U)SIM or any combination thereof. The ME may optionally be personalized to multiple Networks, Network Subsets, Service Providers, Corporate, (U)SIMs or any combinations thereof.

For each of the five Personalisation categories, the ME Personalisation Information includes:

- One or more Personalisation codes, that will be checked against the information stored on the inserted (U)SIM card
- A Personalisation flag (or indicator) that indicates whether ME Personalisation is activated or not, i.e. whether the ME is SIM-Locked or not to this Personalisation category

- A key (the Control Key (CK)) used as the password for Personalisation de-activation, or parameter(s) derived from the CK, for example the hash of the CK
- Stateful data (e.g. retry counter) for protection against dictionary attacks on the CK

The following requirements refer to the all five possible forms of ME Personalisation.

- **ME Personalisation Process:** The process of storing ME Personalisation Information in the ME, and activating the SIM-Lock Mechanism, which verifies this information against the corresponding information stored in the (U)SIM, in order to limit the (U)SIMs with which the ME will operate.
- **ME De-Personalisation Process:** The process of disabling or replacing the old ME Personalisation Information with new information.
- **ME De-Personalisation Mechanism:** The mechanism in charge of the ME De-Personalisation: it receives the de-Personalisation password for a given Personalisation category, compares it to the CK for this Personalisation category, and if they match, the Personalisation flag contained in the ME Personalisation Information is changed and the ME is no longer SIM-Locked to this Personalisation category.
- **SIM-Lock Mechanism:** The mechanism in charge of the verification of the ME Personalisation Information against the corresponding information stored in the (U)SIM, in order to apply the relevant SIM-Lock policy.

9.2 SIM LOCK REQUIREMENTS

PROTECTION OF ME PERSONALISATION INFORMATION:	
REQ. ID	REQUIREMENT
SL 1	<p>The CK included in every Personalisation category SHALL be pseudo-unique per ME. By pseudo-unique, it is meant that:</p> <ul style="list-style-type: none"> According to 3GPP TS 22.022 V6.0.0 [5] section 14, the CK SHALL be decimal strings with an appropriate number of digits for the level of Personalisation. <p>The CK values SHALL be generated randomly or pseudo-randomly such that all possible combinations of digits are equally likely to be generated. There SHALL NOT be any involvement of ME data in the generation of CK values.</p>
SL 2	The CK included in every Personalisation category SHALL be bound to the ME.
SL 3	<p>ME Personalisation-Control Keys SHALL be stored in one of the following locations</p> <ul style="list-style-type: none"> Secure HW HW-Controlled Secure Memory Closed/Secure OS-Controlled Secure Memory. In this case the keys used in providing this cryptographic protection SHALL be stored in Secure HW or in HW-Controlled Secure Memory.
SL 4	<p>ME Personalisation Information with the exception of Control Keys SHALL be stored in one of the following locations:</p> <ul style="list-style-type: none"> Integrity-Protected HW HW-Controlled Integrity-Protected Memory Closed/Secure OS-Controlled Integrity-Protected Memory.

PROTECTION OF ME PERSONALISATION INFORMATION:	
REQ. ID	REQUIREMENT
SL 5	At boot-time, whenever a SIM/USIM is inserted, and prior to any attempt to launch the ME De-Personalisation Mechanism, the ME SHALL verify the authenticity, integrity and binding to the ME of the ME Personalisation Information.
SL 6	<p>The write access to the ME Personalisation Information and especially to the Personalisation flag of each Personalisation category SHALL be controlled and executed in the following manner:</p> <ul style="list-style-type: none"> • In the case where it does not manipulate secrets, the write access mechanism SHALL be either: <ul style="list-style-type: none"> ○ Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Protected Memory, OR ○ a HW-Protected SW executing from and using HW-Controlled Integrity-Protected Memory. • In the case where it manipulates secrets, the write access mechanism SHALL be either: <ul style="list-style-type: none"> ○ a Closed/Secure OS-Protected SW executing from Closed/Secure OS-Controlled Integrity Protected Memory and using Closed/Secure OS-Controlled Secure Memory, OR ○ a HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory.

DETECTION AND REACTION TO ME PERSONALISATION INFORMATION MODIFICATION:	
REQ. ID	REQUIREMENT
SL 7	Unless ME Personalisation Information is stored in Secure HW or in HW-Controlled Secure Memory the ME SHALL detect at boot-time and at run-time any modification that has been made of the ME Personalisation Information as well as of the binding of the ME Personalisation Information with the ME.
SL 8	If the ME Personalisation Information or the binding of the ME Personalisation Information with the ME has been tampered with, before boot-time or at run-time, the ME SHALL NOT be allowed to make any phone call nor any other network connection.

DE-PERSONALISATION PROCESS:	
REQ. ID	REQUIREMENT
SL 9	It SHALL be possible to de-personalize the ME with a keypad entry. If there is no keypad, then an alternative ME-based solution SHALL be provided.
SL 10	It SHALL be possible to de-personalize the ME over-the-air by the network (point-to-point (PP) SMS).
SL 11	The ME SHALL remain personalized if incorrect de-Personalisation code/secret is entered during the de-Personalisation cycle.
SL 12	All possible ME Personalisation categories SHALL be independent so each category can be activated or de-activated regardless of the status of the others.

DE-PERSONALISATION MECHANISM:	
REQ. ID	REQUIREMENT
SL 13	<p>In the case where it does not manipulate secrets, the De-Personalisation Mechanism SHALL be either:</p> <ul style="list-style-type: none"> • an Integrity-Protected HW, OR • a Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Protected Memory, OR • a HW-Protected SW executing from and using HW-Controlled Integrity-Protected Memory. <p>In the case where it manipulates secrets, the De-Personalisation Mechanism SHALL be either:</p> <ul style="list-style-type: none"> • a Secure HW, OR • a Closed/Secure OS-Protected SW executing from Closed/Secure OS-Controlled Integrity-Protected Memory and using Closed/Secure OS-Controlled Secure Memory, OR • a HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory.
SL 14	<p>Unless De-Personalisation Mechanism is Integrity-Protected HW or Secure HW or is stored in HW-Controlled Integrity-Protected Memory or HW-Controlled Secure Memory, the ME SHALL check the authenticity and integrity of the De-Personalisation Mechanism at boot time following the requirements in section 11 "Secure Boot Requirements".</p>
SL 15	<p>Unless De-Personalisation Mechanism is stored in Secure HW or in HW-Controlled Secure Memory, the ME SHALL detect at boot-time and SHOULD detect at run-time, any modification of the De-Personalisation Mechanism by Non-Authorized SW.</p>

ACCESS CONTROL TO THE ME DE-PERSONALISATION MECHANISM:	
REQ. ID	REQUIREMENT
SL 16	It SHALL not be possible to de-personalize the ME for any Personalisation category, without proper authentication information (i.e. CK).
SL 17	The De-Personalisation Mechanism SHOULD either <ul style="list-style-type: none"> - only be accessible to Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Checked Memory, OR - be controlled and restricted to a HW-Protected SW executing from and using HW-Controlled Integrity-Checked Memory.

SIM-LOCK MECHANISM:	
REQ. ID	REQUIREMENT
SL 18	Unless SIM-Lock Mechanism is Integrity-Protected HW or Secure HW or is stored in HW-Controlled Integrity-Protected Memory or HW-controlled Secure Memory, the ME SHALL check the authenticity and integrity of the SIM-Lock Mechanism at boot-time following the requirements in section 11 "Secure Boot Requirements".
SL 19	Unless SIM-Lock Mechanism is stored in Secure HW or in HW-Controlled Secure Memory, the ME SHALL detect, at boot-time and SHOULD detect at run-time, modifications of the SIM-Lock Mechanism by Non-Authorized SW.
SL 20	If the SIM-Lock Mechanism failed in its verification of the SIM-Lock policy, the ME SHALL NOT be allowed to make any phone call nor any other network connection except emergency calls.

SIM-LOCK MECHANISM:	
REQ. ID	REQUIREMENT
SL 21	The Personalisation check SHALL be carried out at boot time, as described in 3GPP TS 22.022 V6.0.0 [5] and SHALL also be carried out after the ME has attached to the cellular network. For the second Personalisation check, the ME SHALL use the value of the IMSI that was used for network attachment and SHALL not read a fresh value of the IMSI from the (U)SIM for the purposes of the second Personalisation check.

REACTION TO MODIFICATION:	
REQ. ID	REQUIREMENT
SL 22	If the ME Personalisation Information, the binding of the ME Personalisation Information with the ME, the De-Personalisation Mechanism or the SIM-Lock Mechanism have been tampered with, before boot-time or at run-time, the ME SHALL NOT be allowed to make any phone call nor any other network connection.

10 DRM REQUIREMENTS

This section defines security requirements, applying to the UE, regarding DRM. This applies to UEs that support DRM.

This document does not imply or recommend adoption of any particular DRM schemes. It defines enablers to be used by the DRM engine.

Definitions:

- **DRM Agent:** An entity in the UE that controls use and protection of DRM-related keys (such as Device-specific keys, domains keys, Rights Object protection keys, Content Encryption Keys) and Rights Objects (and related counters, timers and bindings) on the UE.

REQ. ID	REQUIREMENT
<p>DRM 1</p>	<p>Secure boot and platform integrity:</p> <p>Unless the DRM Agent is implemented in Integrity-Protected HW, then the authenticity and integrity of the DRM Agent and of DRM-related cryptographic software SHALL be verified either at boot time or before the first use after boot time following the requirements in section 11 "Secure Boot Requirements".</p>
<p>DRM 2</p>	<p>Storage of DRM-related keys:</p> <p>The confidentiality, integrity and authenticity of all DRM-related keys (Device-specific keys, domains keys, Rights Object protection keys, Content Encryption Keys) SHALL be protected when not in use. Therefore they SHALL be</p> <ul style="list-style-type: none"> • stored in Secure HW, OR • stored in HW-Controlled Secure Memory, OR • cryptographically protected for integrity and confidentiality if stored in Non-Secure Memory. In this case the keys used in providing this cryptographic protection SHALL be stored in Secure HW or in HW-Controlled Secure Memory

REQ. ID	REQUIREMENT
<p>DRM 3</p>	<p>Usage of DRM-related keys:</p> <p>All DRM-related keys that are provisioned to the ME or (U)SIM during the manufacturing process (e.g. Device-specific keys or keys used to protect short-term DRM-related keys) SHALL be used by either</p> <ul style="list-style-type: none"> • Secure HW, OR • HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory, OR • Closed/Secure OS-Protected SW executing from Closed/Secure OS-Controlled Integrity-Protected Memory and using Closed/Secure OS-Controlled Secure memory. <p>During use, these keys SHALL be passed encrypted to the Secure HW and/or to the Protected SW and only exist in the clear when in the Secure HW and/or Secure Memory.</p> <p>All DRM-related keys that are provided to the ME or (U)SIM after the manufacturing process is completed SHALL be used by Secure HW or Protected SW executing from Integrity-Protected Memory and using Secure Memory. These keys SHALL be passed encrypted to the Protected SW and only exist in the clear when in the Secure HW and/or Secure Memory.</p>
<p>DRM 4</p>	<p>Execution of DRM programme code:</p> <p>All sensitive DRM programme code excluding code manipulating DRM-related keys SHOULD be either</p> <ul style="list-style-type: none"> • Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Protected Memory, OR • HW-Protected SW executing from and using Hardware-Controlled Integrity-Protected Memory.

REQ. ID	REQUIREMENT
DRM 5	Storage of Rights Objects: The authenticity and integrity of Rights Objects and related counters, timers and binding SHALL be protected. If not cryptographically protected, they SHALL either be stored within Integrity-Protected HW or within Integrity-Protected Memory. Any Content Encryption Keys, stored in, and used along with Rights Objects SHALL be protected as described in requirements DRM 2 and 3.
DRM 6	Storage of Content: Confidentiality of content SHALL be protected when not in use. For instance content should be cryptographically protected for confidentiality when stored in Non-Secure Memory.
DRM 7	Content processing software: SW that has access to DRM-protected content in unencrypted form SHALL be Protected-SW.

11 SECURE BOOT REQUIREMENTS

This section defines security requirements applying to the secure boot procedures.

Definitions:

Secure Boot Process: Set of operations, started upon ME initialization, and used to perform hierarchical verification of code's security properties, followed by its execution.

Secure Boot Chain: Combination of a set of one or more Secure Boot Components.

Secure Boot Component: Component used to execute a set of one or more operations of the Secure Boot Process.

REQ. ID	REQUIREMENT
SB 1	<p>Where a SW component is required by this specification to be verified for integrity and authenticity as part of the Secure Boot Process, all other components on which its authenticity and integrity depends, and all components that could compromise its security whose functionality it uses at run time, SHALL themselves also be verified for integrity and authenticity.</p> <p>Each SW component whose integrity and authenticity requires verification SHALL be verified prior to its use.</p> <p>Components in HW-Controlled Integrity-Protected Memory are considered to be verified.</p>
SB 2	The authenticity and integrity of the code handling the Secure Boot Process SHALL be guaranteed.
SB 3	The Secure Boot Process shall be initiated by a software (called initial component) implemented in HW-Controlled Integrity-Protected Memory in the SOC.
SB 4	It SHALL NOT be possible for the Secure Boot Process to be bypassed by any attack considered in the scope of the threat model.

REQ. ID	REQUIREMENT
<p>SB 5</p>	<p>The Secure Boot Process SHALL guarantee, at least:</p> <ul style="list-style-type: none"> a) Authenticity and Integrity of boot loader b) Authenticity and Integrity of the Mobile Device ID, SW components that report the Mobile device ID, Mobile device ID Protection Mechanism, De-Personalisation Mechanism, SW components that use the De-Personalisation Mechanism, SIMLock mechanism c) Authenticity and Integrity of Operating System Core Loading <p>Verification of the SIM Lock Mechanism and the Mobile device ID protection mechanism SHALL be done by HW-Protected SW executing from HW-Controlled Integrity-Protected Memory and using HW-Controlled Secure Memory, if values requiring confidentiality are involved, or HW-Controlled Integrity-Protected Memory, if values requiring confidentiality are not involved.</p>
<p>SB 6</p>	<p>Secure Boot Chain:</p> <p>The Secure Boot Chain MAY employ multiple SW components, the secure Boot Components, each of which is verified for integrity and authenticity by a preceding component.</p>
<p>SB 7</p>	<p>Secure Boot Components (no confidentiality):</p> <p>If no values requiring confidentiality are involved in verifying integrity and authenticity, Secure Boot Components other than the initial component SHALL be either</p> <ul style="list-style-type: none"> • Closed/Secure OS-Protected SW executing from and using Closed/Secure OS-Controlled Integrity-Protected Memory, OR • HW-Protected SW executing from and using HW-Controlled Integrity-Protected Memory.

REQ. ID	REQUIREMENT
SB 8	<p>Secure Boot Components (confidentiality):</p> <p>If values requiring confidentiality are involved in verifying integrity and authenticity, Secure Boot Components other than the initial component, SHALL be either</p> <ul style="list-style-type: none"> • Closed/Secure OS-Protected SW executing from Closed/Secure OS-Controlled Integrity-Protected Memory and using Closed/Secure OS-Controlled Secure memory, OR • HW-Protected SW executing from HW-Controlled integrity-protected Memory and using HW-Controlled Secure Memory.
SB 9	<p>Secure boot chain hardware requirements</p> <p>If Bluetooth, IrDA, RFID, NFC, 802.11 or any other local interface supported by the ME is enabled, the Secure Boot Process SHALL NOT execute any SW components or commands received through that local interface unless and until they have been verified for integrity and authenticity.</p>
SB 10	<p>Where an ME contains multiple processors, each processor shall meet one of the following conditions:</p> <ul style="list-style-type: none"> • The processor SHALL implement all of the Secure Boot Requirements • The processor SHALL only execute code which has already been validated by another processor which implements all of the Secure Boot Requirements <p>ME processors may be excluded from this requirement if it can be shown that a compromise of the processor cannot impact on the implementation and security of any of the other requirements in this document. For example an isolated I/O controller chip which has its own processor running either from ROM or from its own non-volatile storage and which is accessed solely by an external bus could be excluded.</p>

12 SECURE BINDING REQUIREMENTS

This section considers security requirements applying to the secure binding between ME and (U)SIM.

Specifications required to implement the requirements in this section are not currently available. The requirements in this section will not apply until such specifications are available from the respective SDOs or initiatives. It is currently anticipated that OMTP is going to consider the following two requirements discussing and agreeing the proper references once they are available.

The term secure binding refers to the term secure channel in other standards (TCG - TCP Mobile Phone Group use cases document), OMA, 3GPP, ETSI/SCP - document TS 102 412).

A secure channel is a method or technique assumed to provide means by which data can be transferred from (U)SIM to ME (or ME to (U)SIM) without risk of interception or tampering.

REQ. ID	REQUIREMENT
SG 1	After or during the secure boot process the ME and (U)SIM SHOULD perform a unilateral or mutual authentication called <i>secure binding</i> to build up a secure communication channel.
SG 2	If a secure communication channel is in place, the ME and (U)SIM SHALL guarantee the unilateral or mutual authenticity, integrity and/or confidentiality of communications between (U)SIM and ME.

13 SECURE FLASH UPDATE REQUIREMENTS

This section defines security requirements applying to the secure code download process.

The purpose of the secure code download process is to provide a mechanism by which authorized parties can install code updates into the non-volatile storage of the ME using the local interfaces of the ME. Typically serial ports or USB ports are used for this purpose. This mechanism could be used to recover terminals which have been rendered inoperable by external failures (e.g. cosmic rays affecting the flash) or where new software versions are to be installed. Not all devices and operating systems support this mechanism.

For example a mechanism by which this can be achieved is that at boot time the boot code detects from signals on the hardware interface that a secure code download is being requested. At this point a small program is downloaded over this interface which is checked for authenticity and integrity before it is executed. This program then carries out the remainder of the flash download process: it must verify the integrity and authenticity of all code which is downloaded.

REQ. ID	REQUIREMENT
SF 1	The secure flash update process SHALL be initiated by software executing from and using HW-Controlled Integrity-Protected Memory.
SF 2	The software handling the secure flash update process SHOULD be a HW-Protected SW executing from and using HW-Controlled Integrity-Protected Memory.
SF 3	It SHALL NOT be possible for the secure flash update process to be bypassed by any attack considered in the scope of the threat model, to be sure the flash loader SW is authenticated before any subsequent SW execution.
SF 4	Unless the software handling the secure flash update process is stored in Integrity-Protected HW or in HW-Controlled Integrity-Protected Memory, it SHALL be verified at boot time before its execution following the requirements in section 11 "Secure Boot Requirements".
SF 5	The secure flash download mechanism SHALL ensure the authenticity and integrity of all code which is downloaded before execution on the device.

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